High-aspect-ratio chemically assisted ion-beam etching for photonic crystals using a high beam voltage-current ratio

M. V. Kotlyar,[a] L. O'Faolain, R. Wilson, and T. F. Krauss
Ultrafast Photonics Collaboration, School of Physics and Astronomy, University of St. Andrews, St. Andrews, Fife KY16 9SS, Scotland, United Kingdom

(Received 18 December 2003; accepted 5 May 2004)

We investigate etching conditions for photonic crystals (PhCs) in InGaAsP/InP and AlGaAs/GaAs using a new regime of CAIBE operation. We show that the beam voltage-current ratio is critical in obtaining high material/mask selectivity. For one-dimensional PhCs, i.e., air slots, selectivities of 22:1 and 50:1 were achieved in InP and GaAs, respectively, using a very high beam voltage (about 1500 V) and a low beam current (about 10 mA). Etched features were observed to be very smooth, i.e., edge roughness was low. Two-dimensional PhCs were etched in InGaAsP/InP under similar conditions achieving selectivities up to 27:1 and 34:1 for hole diameters of 170 and 270 nm, respectively. © *2004 American Vacuum Society.* [DOI: 10.1116/1.1767106]

PROOF COPY 023404JVB

I. INTRODUCTION

Photonic crystal devices have many possible applications in telecommunications and other industries due to their ability to control the flow of light on a wavelength scale. Because photonic crystals are based on a periodic high-contrast refractive index modulation, high-quality fabrication techniques are of paramount importance for the realization of useful devices.

Chemically assisted ion-beam etching (CAIBE) is rapidly proving itself, with inductively coupled plasma (ICP) etching,[1] to be one of the most effective etching processes. It has advantages over similar techniques, such as reactive ion etching (RIE), because it gives independent access to the plasma generation and etching conditions, thereby enabling better control over the etching process. This independent control is critical for the etching of high-aspect-ratio features, as we will demonstrate below.

High-quality GaAs etching has already been achieved,[2] whereas InP etching is yet to be developed to the same level. InP etching typically produces tapered holes,[3] whereby the taper compromises device performance. In addition, InP/InGaAsP heterostructures typically have lower confinement due to the lower refractive index contrast. So the mode is further extended vertically, which leads to a larger vertical extent of the mode and the requirement of a greater depth when etching InP.

In this paper, we etch GaAs/AlGaAs and InP/InGaAsP "laser-like" wave guiding heterostructures using a new regime of CAIBE operation.

II. CONDITIONS FOR BALANCED ETCHING PROCESS

In CAIBE etching of III–V semiconductors, chlorine is typically used. Chlorine reacts with the group III elements forming volatile byproducts, such as $GaCl_3$, $InCl_3$, and others. This reaction does not take place spontaneously, but needs an activation energy, which is supplied by an argon ion beam. To produce photonic crystal features with a high aspect ratio, the effects of physical and chemical etching must be carefully balanced. The reaction between InP and chlorine has a threshold temperature of 140 °C–190 °C.[4] As a result, we heat the sample up to 185 °C. This temperature is sufficient to allow the chemical etching to counterbalance the physical etching.

Pattern definition requires the use of a mask, usually SiO_2 or SiN_x. The mask does not react with the chlorine but is eroded by the physical impact of the high-energy argon ions.

In our fabrication progress, the desired design is written in a polymethylmethacrylate (PMMA) mask using electron beam lithography. The pattern is then transferred into the silica mask using RIE with fluorine chemistry.

Figure 1(a) shows etching results for an InP-based sample. A temperature of 185 °C, 30 mA beam current, 900 V beam voltage, and 0.9 sccm Cl_2 flow was used. These conditions lead to a physically dominant etching process. This causes an overcut wall profile with widening at the top of the hole and a poorly formed hole bottom. By increasing the Cl_2 flow up to 1.6 sccm and, further, the chemical and physical components of the etching process should become better balanced. However, we never managed to achieve a satisfactory profile with these conditions, as even when chemical and physical components are balanced, another problem, "bending," may occur (also reported by Ferrini *et al.*[3]).

For high-quality, high-aspect-ratio etching, a different solution is therefore required. To this end, we modified the physical etching conditions.

In Fig. 1(b), we reduced the beam current from 30 to 12 mA and increased the beam voltage from 900 to 1200 V, thus entering a much more favorable etching regime. It appears that a higher voltage gives a stronger directionality to the etching process, thereby minimizing the tendency to etch sideways, which causes such a "bend." The feature shown in Fig. 1(b) is a one-dimensional PhC in InP-based material with air slots of 90 nm and an etch depth of 3.5 μm (aspect ratio of 38:1).

[a]Electronic mail: mvk@st-andrews.ac.uk

PROOF COPY 023404JVB

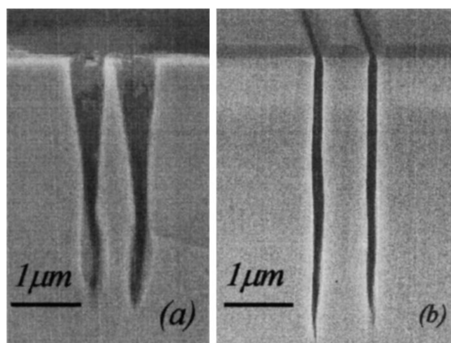

FIG. 1. SEM (scanning electron microscope) images of one-dimensional features of 90-nm size in InP-based material: (a) physically dominant etching process; (b) a good chemical–physical balance; a 38:1 aspect ratio was achieved with mask selectivity of 18:1.

For GaAs etching, a lower temperature is used (typically 120 °C), but otherwise, the same principles apply. In our experience, the margins for error in etching high verticality features are larger in GaAs than in InP, and the general quality is somewhat better (it is very rare to observe bending or wobbling in GaAs features, and tapering toward the bottom of the hole is more easily cured).

III. SEMICONDUCTOR/MASK SELECTIVITY

Once the process is correctly balanced, the main factor limiting the achievable depth of the etched holes is the mask etch rate relative to the material etch rate, i.e., the mask selectivity.

In Fig. 2, we show the relationship between the mask selectivity and the beam voltage. In this graph, we only plot points corresponding to a balanced etching process. As can be seen, these points lie approximately on a straight line and fulfill the condition of constant beam power, i.e., a constant beam voltage-current product. For such constant beam power and balanced etching, a mask selectivity as high as 50:1 was achieved in AlGaAs/GaAs for air slots with a slot width of 100 nm. These conditions also enabled us to etch air slots as small as 60 nm in width to a depth of 1.2 μm, i.e., with an aspect ratio of 20:1.

To understand this increase in selectivity with beam voltage, we need to examine both the etch rate of the III–V material and that of the silica mask.

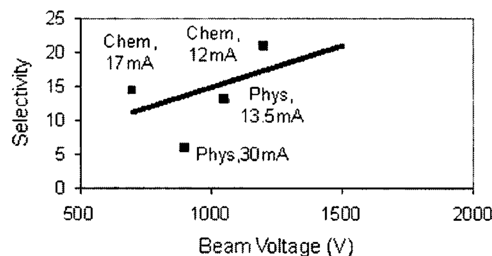

FIG. 3. The selectivity of chemically overetched and physically overetched holes with respect to an "in-balance" line (InP etching).

The silica mask etch rate is constant for a given beam voltage and current, i.e., it is independent of the chemical etching component, because it does not react with the chlorine. The III–V material etch rate, on the other hand, is strongly dependent on the chemical etch conditions (chlorine flow and temperature). Thus, the selectivity of chemically overetched features lies above the balanced line and that of chemically underetched (physically overetched) features lies below (Fig. 3).

We believe that the observed improvement in selectivity for etching at a high voltage-current ratio is due to a hardening of the mask under the impact of high-energy ions. Figure 4 shows a significant reduction in the silica mask etch rate with increasing beam voltage. We have also observed that the remaining silica mask after a CAIBE etch is more resistant to RIE than before. We assume that this hardening simply occurs as a consequence of the ion impact. The equivalent graph for the semiconductor, i.e., etch rate versus beam voltage, is approximately flat. Due to the strong dependence of the semiconductor etch rate on the physical–chemical balance, it is difficult to determine the semiconductor etch rate exactly, making a direct comparison between the two etch rates problematic.

What is clear, however, is that the selectivity increases with the beam voltage when the etch conditions are on the "balanced" line, as shown in Figs. 2 and 3.

We also observe that the etch rate (and selectivity) decreases with decreasing feature size (see Fig. 5). This is a well-documented phenomenon that is believed to be a form of RIE lag.[5]

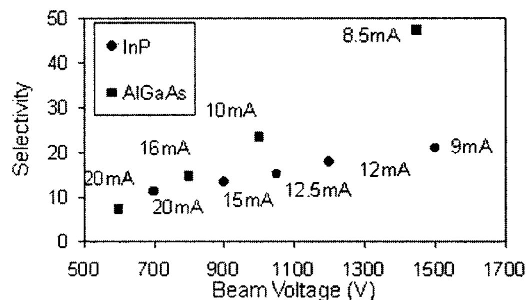

FIG. 2. The dependence of the semiconductor/mask selectivity on the beam voltage-current ratio for InGaAsP/InP and AlGaAs/AlAs materials.

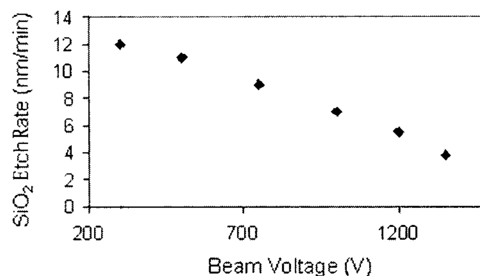

FIG. 4. The dependence of the silica mask etch rate on the beam voltage. Beam current, temperature, and chlorine flow were kept the same.

PROOF COPY 023404JVB

PROOF COPY 023404JVB

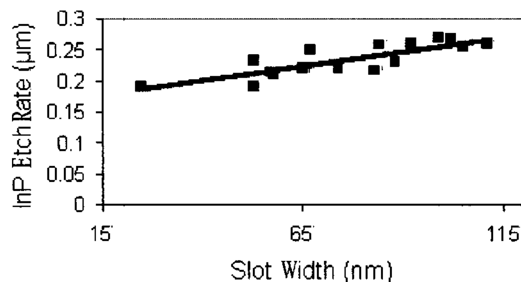

FIG. 5. The dependence of the InP etch rate on the hole size under optimized etching conditions. All measurements are taken from the same sample.

IV. "NECK" FORMATION

The formation of a "neck"[5] just below the surface in InP etching was observed at times (see Fig. 6). "Neck" formation takes place when the chemical component of the etching process is slightly dominant. The increased surface temperature due to heating by the ion beam, coupled with the effects of ions ricocheting off the mask edges, increases the anisotropic etch rate in the vicinity of the surface. Even a small deviation from a good "chemical–physical" balance is enough for such a "neck" to be formed. The higher the amount of Cl_2 or the substrate temperature (with the rest of the parameters unchanged), the bigger a "neck" is observed. In accordance with this argument, the "neck" shown in Fig. 6 could be easily removed by increasing the beam current from 8.5 to 9 mA (for a beam voltage of 1500 V), thus slightly increasing the amount of physical etching and returning to the perfect "physical–chemical" balance. This feature is rarely observed in GaAs.

V. LOW SIDEWALL ROUGHNESS

One of the concerns with CAIBE is that the high ion energies lead to more violent impacts, resulting in increased sidewall roughness. We did not observe any such behavior for the conditions described here.

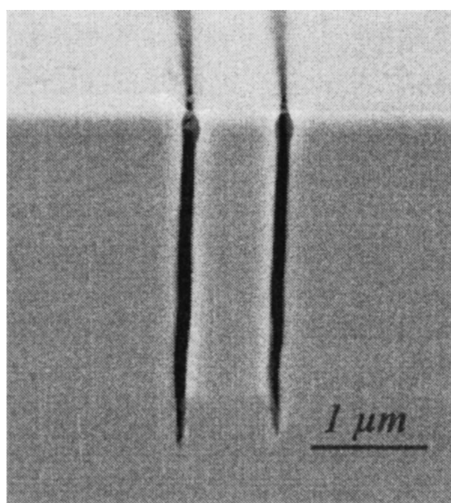

FIG. 6. A 100-nm feature size etched in InP-based material. The "neck" observed at the top of the hole is due to a small "chemical–physical" unbalance.

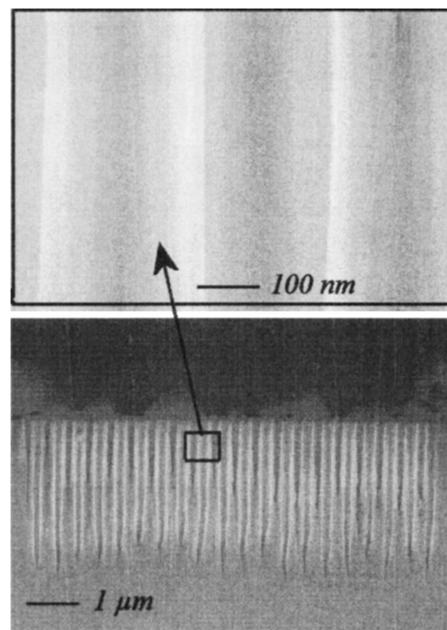

FIG. 7. SEM images of a PhC (enlarged image at top) etched under high-voltage conditions demonstrating a low level of sidewall roughness. The etching depth was 3.7 μm (a hole diameter of 195 nm).

In our case, due to the low beam current, we believe that there is a large ion-induced chemical-etching yield. The initial impact of an ion causes roughness, which is then largely erased by the chlorine, which reacts faster in the region of the impact due to the localized heating caused by the ion impact. An enlarged image of an etched PhC in Fig. 7 shows low sidewall roughness. Furthermore, the low measured propagation losses of PhC devices etched using high beam voltage and low current proves that sidewall roughness was not high.[6] This agrees qualitatively with the results of Daleiden *et al.*,[7] who show that CAIBE causes less damage than IBE. Thus, by extension, it is plausible that a strong chemical component may reduce damage caused by the physical component.

VI. ETCHING OF PHOTONIC CRYSTALS

InGaAsP/InP and AlGaAs/GaAs two-dimensional photonic crystals have also been etched successfully using these guidelines. GaAs-based PhCs were etched to a depth of 1.6 μm with a mask/semiconductor selectivity of 32:1 for a hole diameter of 200 nm. InP/SiO_2 mask etching ratios of 27:1 and 34:1 were achieved for 170- and 270-nm diameter holes, respectively, with corresponding hole depths of 3.5 and 4.4 μm, i.e., aspect ratios of 21:1 and 16:1. The etching was done for the same conditions as used for air slots (1200 V, 12 mA, 1.6 sccm Cl_2, 185 °C). Propagation losses as small as 1.8–3.5 dB/mm were measured for planar PhC wave guides in InP-based material etched under these conditions. These PhCs were etched to the depth of 5.3 μm (Fig. 8). To date, these are the best-reported results for etching InP-based PhCs.[8]

PROOF COPY 023404JVB

PROOF COPY 023404JVB

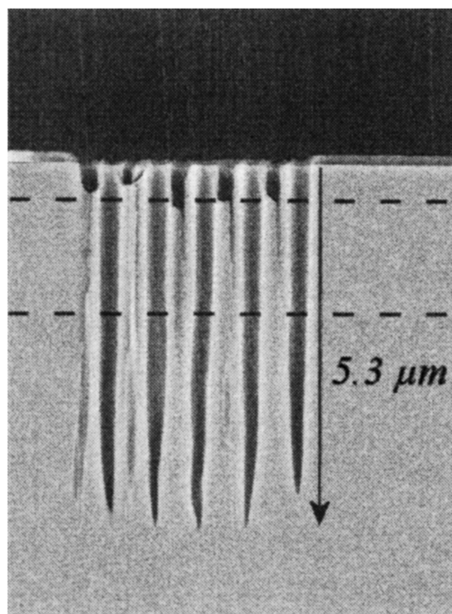

FIG. 8. A SEM image of extremely deep PhCs etched in InGaAsP/InP material. The hole diameter is 250 nm. Losses of 1.8–3.5 dB/mm were measured for this sample. The dashed lines have been added to highlight the position of the wave guiding layer (1.58 μm thick).

VII. CONCLUSIONS

We have examined a new regime of CAIBE operation. We discussed the consequences of a ''chemical–physical'' unbalanced etching process and found that this balance is achieved for an approximately constant beam power, i.e., beam voltage-current product. The selectivity of the etch process increases with increasing beam voltage/current ratio, due to an increased mask resistance to high-energy ions. The high mask selectivity allows us to use a relatively thin silica mask (200–300 nm) that can be patterned with high resolution and good control over feature sizes. This regime can be used both for InP- and GaAs-based photonic crystal etching because no increase in sidewall roughness is observed, even at high-voltage etching conditions. Therefore, we were able to take advantage of the increased directionality of high beam voltage etching to produce high-quality InP-based photonic crystals with an etch depth of up to 5.3 μm.

ACKNOWLEDGMENTS

We would like to thank Mr. George Robb and Dr. Lijun Wu for their help with experiments and useful discussions. This work was supported by EPSRC and the Scottish Higher Education Funding Council (SHEFC).

[1]R. Ferrini, B. Lombardet, B. Wild, R. Houdre, S. Olivier, H. Benisty, A. Djoudi, L. Legouezigou, S. Hubert, S. Sainson, J.-P. Chandouineau, S. Fabre, F. Pommereau, and G.-H. Duan, Electron. Lett. **38**, 962 (2002).
[2]K. Avary, J. P. Reithmaier, F. Klopf, T. Happ, M. Kamp, and A. Forchel, Microelectron. Eng. **61–62**, 875 (2002).
[3]R. Ferrini, D. Leuenberger, M. Mulot, M. Qui, J. Moosburger, M. Kamp, A. Forchel, S. Anand, and R. Houdre, IEEE J. Quantum Electron. **38**, 786 (2002).
[4]K. Asakawa, T. Yoshikawa, S. Kohmoto, and Y. Nambu, Jpn. J. Appl. Phys. **37**, 373 (1998).
[5]M. Mulot, S. Anaud, C. F. Carlstrom, M. Swillo, and A. Talneau, Phys. Scr. **T101**, 106 (2002).
[6]M. V. Kotlyar, T. Karle, M. D. Settle, L. O'Faolain, and T. F. Krauss, Appl. Phys. Lett., to be published.
[7]J. Daleiden, R. Keifer, S. Klussmann, M. Kunzer, C. Manz, M. Wailher, J. Braunstein, and G. Weimann, Microelectron. Eng. **45**, 9 (1999).
[8]M. Mulot, M. Qui, M. Swilo, B. Jaskorzynska, S. Anaud, and A. Talneu, Appl. Phys. Lett. **83**, 1095 (2003).

PROOF COPY 023404JVB

PROOF COPY 023404JVB