

Low loss silicon on insulator photonic crystal waveguides made by 193nm optical lithography

Michael Settle¹, Mike Salib², Albert Michaeli³ and Thomas F. Krauss¹

¹ University of St Andrews, St Andrews, Fife, KY16 9SS UK

² Intel Corporation, 2200 Mission College Blvd, Santa Clara, CA 95054 USA

³ Intel Corporation, Kyriat Gat, 82109, Israel

tfk@st-and.ac.uk

Abstract: We show the successful fabrication and operation of photonic crystal waveguides on SOI, with lower silicon dioxide cladding remaining, using 193 nm DUV lithography. We demonstrate that 193 nm lithography gives more process latitude, allowing a wider range of periods and hole diameters to be printed, as well as reducing the optical proximity effect to a minimum. The smallest period /hole size variation printed successfully was 280 nm and 150 nm, which is very promising for ambitious future designs. Lowest losses obtained were 14.2 ± 2.0 dB/cm for a W1 waveguide in a 400 nm lattice with an r/a of 0.25 at a frequency of $0.257 a/\lambda$, which approaches the best losses reported for air-bridge type W1s.

©2006 Optical Society of America

OCIS codes: (230.7370) Waveguides; (220.4610) Optical fabrication; (250.5300) Photonic integrated circuits.

References and links

1. M. Notomi, A. Shinya, S. Mitsugi, E. Kuramochi, and H. Ryu, "Waveguides, resonators and their coupled elements in photonic crystal slabs," *Opt. Express* **12**, 1551-1561 (2004), <http://www.opticsexpress.org/abstract.cfm?URI=OPEX-12-8-1551>.
2. E. Kuramochi, M. Notomi, S. Hughes, A. Shinya, T. Watanabe and L. Ramunno, "Disorder-induced scattering loss of line-defect waveguides in photonic crystal slabs," *Phys Rev B*, **72**, 161318 (2005).
3. E. Dulkeith, S. J. McNab, and Yu. A. Vlasov, "Mapping the optical properties of slab-type two-dimensional photonic crystal waveguides," *Phys. Rev. B* **72**, 115102 (2005).
4. Y. Akahane, T. Asano, B.-S. Song, and S. Noda, "High-Q photonic nanocavity in a two-dimensional photonic crystal," *Nature* **425**, 944-947 (2003).
5. Yu. A. Vlasov, M. O'Boyle, H. F. Hamann and S. J. McNab, "Active control of slow light on a chip with photonic crystal waveguides," *Nature* **438**, 65-69, (2005).
6. W. Bogaerts, V. Wiaux, D. Taillaert, S. Beckx, B. Luyssaert, P. Bienstman, and R. Baets, "Fabrication of photonic crystals in silicon-on-insulator using 248-nm deep UV lithography," *IEEE J. Sel. Top. Quantum Electron.* **8**, 928 (2002).
7. W. Bogaerts, R. Baets, P. Dumon, V. Wiaux, S. Beckx, D. Taillaert, B. Luyssaert, J. Van Campenhout, P. Bienstman, and D. Van Thourhout, "Nanophotonic waveguides in silicon-on-insulator fabricated with CMOS technology," *J. Lightwave Technol.* **23**, 401-412 (2005).
8. M. Ayre, T. J. Karle, L. Wu, T. Davies, and T. F. Krauss, "Experimental verification of numerically optimized photonic crystal injector, Y-splitter, and bend," *IEEE J. Sel. Areas Commun.* **23**, 1390-1395 (2005).
9. H. Ryu, M. Notomi, G. Kim, and Y. Lee, "High quality-factor whispering-gallery mode in the photonic crystal hexagonal disk cavity," *Opt. Express* **12**, 1708-1719 (2004), <http://www.opticsexpress.org/abstract.cfm?URI=OPEX-12-8-1708>.
10. Yu. A. Vlasov, N. Moll, and S. J. McNab, "Mode mixing in asymmetric double-trench photonic crystal waveguides," *J. Appl. Phys.* **95**, 4538-4544 (2004).

1. Introduction

The miniaturization and mass-manufacture of photonic integrated circuits, with the aim of emulating the success of the microelectronics industry, is one of the key objectives of the field of Silicon Photonics. Silicon-on-Insulator (SOI) material is the preferred platform on which to

build such photonic circuits due to its compatibility with CMOS processing tools and its favorable optical properties at 1.55 μm wavelength. Photonic crystals (PhCs) realized on SOI offer additional opportunities for functional devices within these circuits due to their rich dispersive properties and their ability to strongly confine light. Using e-beam lithography, NTT have reported losses in W1 waveguides of 15dB/cm and 5dB/cm [2] for SiO₂-clad and air-clad devices respectively [1]. IBM has also reported low loss air-clad waveguides (8 ± 2 dB/cm) [3]. High Q cavities [4], and significant reductions in group velocity [5] have now all been realized in SOI-based structures. While these developments clearly underline the potential for ultra compact functional devices, the best results rely on electron-beam lithography and use the theoretically favorable "air-bridge" geometry. In order to comply with mass-manufacturing requirements, optical lithography is preferable and the structures should remain on a solid substrate. In this paper, we report the realization of low loss PhC SOI waveguides fabricated using 193 nm deep-UV (DUV) lithography that fulfill these requirements.

Pioneering work at IMEC, Belgium, using 248 nm DUV lithography, has shown the viability of the DUV process for photonic crystal manufacture [6]. The researchers demonstrated large-scale printing of photonic crystal devices with high fidelity and report losses on W1 SiO₂-clad waveguides of 75dB/cm [7]. Since the requirements for photonic crystal manufacture (approx. 400 nm period structures with 200 nm diameter holes) push 248 nm lithography to its very limits, however, the process window is small and optical proximity correction (OPC) is critical. Moving on to 193 nm lithography should relax the tolerances, allow printing of variable size holes within a circuit (as required for optimized waveguides devices [8] and cavities [9]) and considerably reduce the impact of the optical proximity effect.

W1 waveguides, consisting of a single line of missing holes, are commonly used for assessing the propagation loss and thereby the processing quality of a PhC. Although intrinsically lossless in the regime below the light line where no radiation modes are available, PhC waveguides suffer from wall roughness and non-verticality, randomization of the hole position, size and shape, all of which are lithography and processing related; in fact, they respond very sensitively to any such deviation from the ideal lattice due to the high index contrast ($>3:1$) between the silicon matrix and the air hole lattice. The ultimate loss achievable is therefore technology-limited. Design aspects also play a role, however. Using a solid substrate rather than the air-bridge geometry, while having practical advantages, causes additional mode conversion losses; due to the asymmetry between the silica bottom cladding and the air top cladding, TE and TM modes are no longer decoupled and can interact [10]. Furthermore, operating on an SiO₂ cladding severely reduces the available bandwidth for low-loss operation compared to an air cladding. We demonstrate the limitations imposed by this additional boundary condition.

2. Fabrication

The devices were fabricated on Smart Cut, 8-inch SOI wafers with a 240 nm Si layer on a 2 μm buried oxide (BOx). Etching was carried out using a two stage etch process: the hardmask was etched in a TEL Unity II etcher, and the deeper silicon etching in a Hitachi M511 ECR deep etcher.

For the hard mask etch, C₄F₈/O₂ chemistry was used, whereas the silicon etch was based on HBr/Cl₂ chemistry. The silicon etch recipe was optimized for minimal footing and minimal retrograde sidewall profiles, particularly at the Si/SiO₂ interface. In contrast to air-bridge structures, where the BOx is removed after dry etching, the etch floor is critical to device performance and has to be as square as possible. In addition, there were difficulties etching through the isolated ridge waveguides and the PhC holes simultaneously, because the different pattern densities across the die cause local etch rate variations. The etching process was optimized for the hole profiles and angles of 87-90° were achieved, even for structures with holes down to 150 nm (Fig. 1).

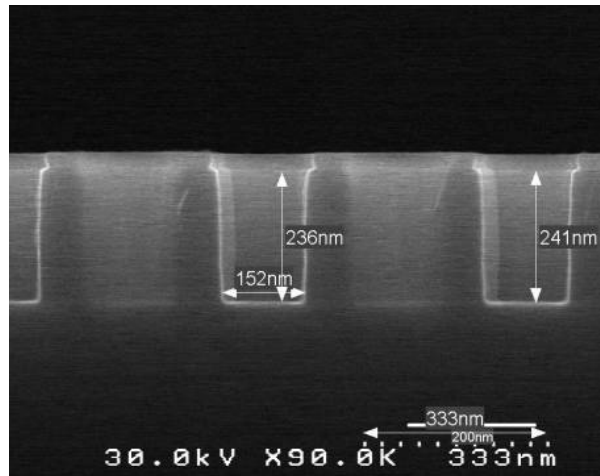


Fig. 1. Cross section of PhC crystal holes, period 280nm and diameter 152nm.

Previous work by Bogaerts et al. at IMEC, Belgium, has highlighted the need to account for optical proximity effects [7]. These are due to optical interferences between neighboring holes, and critically depend on the exposure wavelength and process window. The more the exposure wavefunctions overlap, the stronger the effect. For 248 nm exposure, for example, variations in hole size from 350 nm to 420 nm have been reported [7]. Optical proximity correction (OPC) is needed to pre-compensate for this effect and to ensure that holes situated at exposed places (e.g. corners, borders) are printed at the same size as those in the middle of the lattice. As a starting point for our experiments, we therefore used similar biasing as described by the IMEC-group. The results were surprising, however, as the uncorrected patterns printed using our 193 nm process showed virtually no proximity effect (Fig. 2).

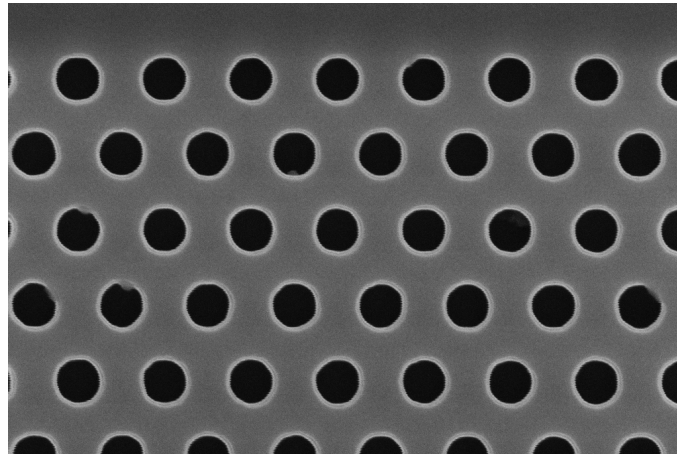


Fig. 2. Top view of a photonic crystal lattice printed without proximity correction using 193 nm lithography. The top line of holes constitutes a row of border holes; where as the rest of the holes can be considered as bulk lattice. Image analysis conducted by fitting a best circle to each hole yielded a size of 194.3 ± 2.3 nm for the border holes, and 195.3 ± 2.0 nm for the bulk lattice holes. The optical proximity effect is therefore smaller than the hole size variation and thus negligible.

3. Optical characterization and results

W1 waveguides were fabricated with a wide range of periods (280nm – 460nm) and hole diameters ($r/a=0.25 - 0.4$). Access waveguides of 5 μm width were used to connect the photonic crystal waveguides to the cleaved facets, using adiabatic tapers. Typical sample length was 5 mm. An Erbium fiber amplified spontaneous emission (ASE) source with $\lambda=1525\text{-}1575$ nm useful wavelength range and an optical spectrum analyzer (OSA) were used to record the output with a resolution of 0.01nm. The light was launched into the access guide using free-space optics. This allowed the launched polarization to be controlled with a polarizer and half-wave plate. An analyzer was placed at the output before the OSA. The propagation loss for the W1 waveguides was calculated using the cut-back method using six lengths of PhC ranging from 30 μm to 1000 μm . For a lattice of $a=400$ nm with an r/a of 0.25, we found a minimum loss of 14.2 ± 2.0 dB/cm at a frequency of $0.257 a/\lambda$ (Fig. 3). Although the insertion loss is of order 10 dB, the repeatability of the transmission measurements was very good. The typical error resulting from the measurement of 6 devices per length resulted in an error of 2dB/cm or better. The loss of the access waveguides was determined, using Fabry-Perot type measurements, to be well below 1 dB/cm and is therefore smaller than the measurement error.

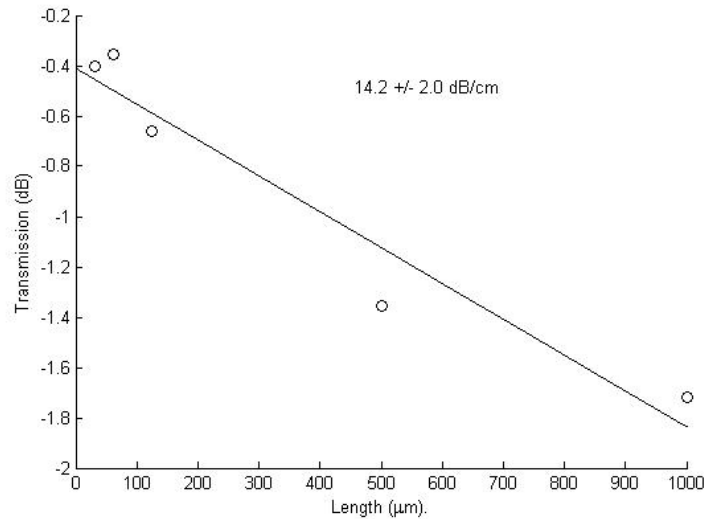


Fig. 3. Propagation loss for W1 PhC waveguide determined by the cut-back method.

Within experimental error, this result is close to the best reported value for e-beam fabricated, but otherwise comparable PhC waveguides [1]. The small bandwidth of the low-loss window is a combination of the light line limitation and the cladding asymmetry caused by the presence of the silica cladding. The bandstructure shown in Fig. 4 highlights the small width of the low-loss window between 0.255 and $0.260 a/\lambda$, corresponding to 30 nm at 1550 nm. This is further reduced by an interaction between the TE and TM-like waveguide modes, which leads to a transmission dip just above the low-loss peak at $0.257 a/\lambda$. Whereas the TE-like mode experiences the photonic bandgap, the TM-like mode is index guided.

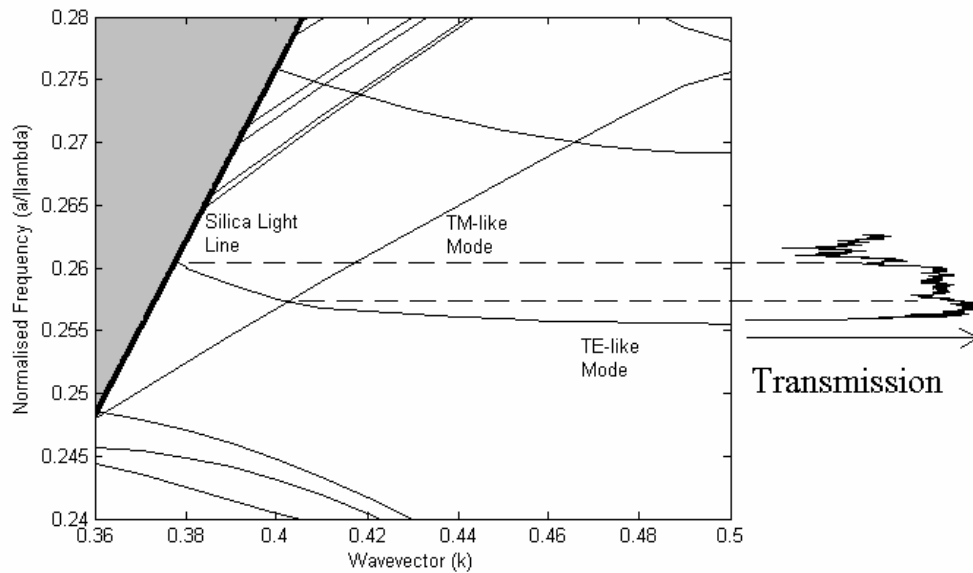


Fig. 4. Bandstructure and corresponding transmission window of the asymmetric oxide-clad W1 waveguide. The spectrum corresponds to the loss determined by the cut-back method across seven lengths.

The TE/TM mode mixing is further confirmed by measurements through crossed polarizers (Fig. 5). For TE excitation and TM detection, we obtain distinct peaks in transmission that correspond to the dips for TE detection. This clearly demonstrates that a degree of polarization conversion takes place in the waveguide.

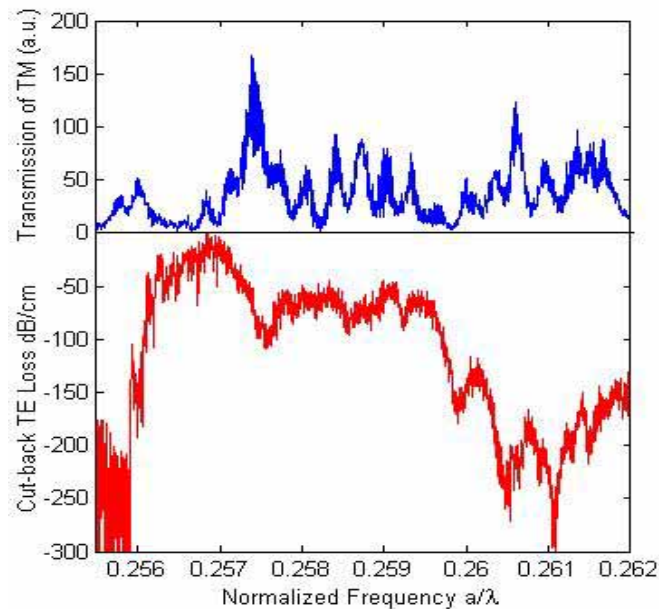


Fig. 5. TE transmission (in dB/cm) and corresponding TM conversion (in arb. units). Both traces were obtained for TE excitation.

4. Conclusion

While the best results with photonic crystal waveguides reported thus far have been obtained with air-bridge type devices, it is worth exploring the alternative of structures with the bottom cladding remaining. Air-silicon-oxide waveguides have clear advantages in terms of manufacturing, integration with non-PhC devices and thermal dissipation. We have found losses in this type of PhC waveguide to be 14.2 ± 2 dB/cm, which corresponds to only a threefold increase compared to the best air-bridge data available. Considering the short size of a typical PhC device, however, this type of loss is clearly acceptable for many applications. The bandwidth of these waveguides is reduced to only a few nm due to a combination of the light line limitation and TE/TM coupling. While the light line limitation can be reduced by using smaller holes [3], the polarization coupling can only be improved by further optimization of the fabrication process, although some of it appears intrinsic due to the inherent asymmetry of the structure.

Fabrication using 193 nm DUV lithography has shown clear advantages over the previously reported 248 nm process, both in terms of process latitude and proximity correction. We have successfully printed periods down to 280 nm with hole sizes as small as 150 nm. Considering that many novel PhC designs incorporate smaller holes to improve functionality, e.g. at bends and Y-junctions, this is a milestone for DUV lithography, and the performance gap to e-beam lithography has been further reduced. The negligible proximity effect demonstrated in Fig. 2 is another major improvement reported, as both e-beam and optical lithography typically suffer from proximity effects that require considerable pre-compensation of the pattern files. The increased process latitude of the 193 nm process has clearly addressed this.

Acknowledgments

The research in this paper was funded through a three-year Strategic Research grant from Intel Corporation.

We thank A. Lazar, H. Bechor, T. Barlavi, A. Bergel, E. Belenky, R. Piliposian, I. Paster for process development support and technical assistance in device fabrications at Intel Fab18 in Kiriath Gat, D. Fishman for SEM X-sections and M. Horev for technical advice. We also acknowledge the effort of Kim Callegari, Jeffrey Tseng and Mohammadumar Piracha in sample preparation, Duc Tran for layout, and finally Ansheng Liu for useful discussions.